Examination Report for the PhD Thesis
"Architecture and protocols for networks-on-chip implemented in FPGA devices"
by Mr. Jakub Siast

The main topic of this thesis is the scientifically investigation and realization of a network-on-chip (NoC) which is optimized for typical FPGA architectures in terms of performance and resource requirements. The realized NoC is called RingNet and consist of a combination of a ring and a tree topology, as this can be constructed using switches with 3-ports. Based on Mr. Siasts investigations those 3-port switches and topology, provide a scalable solution with a low area overhead on FPGAs, as the routing is further simplified. Packet switching based on virtual cut-through is used to transfer packets. An indirect communication based on a system memory (for data packets) and a reflector module (for control packets) at the root of the tree topology is used, in order to provide a solution for determining the buffer size in the NoC. The protocol is based on the OSI layers. With these settings RingNet provides guaranteed throughput, predictable latency and fair network access. Mr. Siast contributes with this work essentially to the scientific work in this domain and provides important concepts and realization alternatives. Mr. Siast evaluated the performance of RingNet using simulations. The resource requirements are evaluated for three different FPGA architectures (Xilinx, Intel and Altera) using synthesis results. The scientific results beat the current state of the art architecture (AXI4 Interconnect) in terms of resources and achievable clock frequency.

The thesis is structured into the following 10 chapters and several appendices:

Chapter 1: Introduction, presents an overview and motivation of the work. Finally, the research objectives and contributions are presented.

Chapter 2: Gives an overview of features and restrictions of current FPGA architectures in respect to ASICs.

Chapter 3: Presents the requirements for FPGA-based NoCs and the current state-of-the-art in this area. Most NoCs are designed for ASIC realizations and only few target FPGA implementations. The most recent ones are referenced and analyzed in this section with a focus on reliability and buffer size adjusting techniques. However, there are also other FPGA-based NoCs that could have been analyzed here. Especially, also other communication infrastructure which focus on a memory-oriented SoC, i.e. most traffic starts and ends in a memory.

Chapter 4: Presents the AXI4 Interconnect as well as other FPGA-based NoCs and crossbars and compares them in terms of cost reduction, distributed RAM utilization, inter-FPGA compatibility, reliability and SDRAM support. The focus here is on the most recent FPGA-based NoC and crossbar solutions. Also here it would have been interesting to also look at other solutions, especially those which use a similar communication scheme via one specific node (SDRAM).

Chapter 5: Gives an overview of the RingNet architecture and presents the key ideas of this dissertation, which include: indirect communication, virtual-cut through switching, 3-port switches, topology combining a ring and a tree structure, throughput control and multiple physical techniques, flit size and flow control.

Chapter 6: Explains in details the realization of all RingNet components and the communication protocol, which is based on the OSI layer model. For the realization decisions of each component, Mr. Siast took into account the investigations described in the previous chapters, in order to find a good solution in terms of a high-performance NoC for FPGA-based systems.

Chapter 7: Presents the simulation results of a RingNet with 2 levels of rings in terms of performance, latency, packet priorization and access fairness. A special case of the permutation traffic pattern is used to resemble the memory-centric SoC traffic pattern of RingNet. It is also briefly mentioned that RingNet was successfully deployed as a communication infrastructure for an FPGA-based depth map estimation system [Dom15]. In my opinion, it is always great to see that aspects and concepts of a thesis also result in a practical realization. It would have been nice, if this would have been described more in detail in the thesis.

Chapter 8: Synthesis results in terms of maximum achievable frequency as well as resource requirements for different FPGA devices from leading vendors (Xilinx, Intel and Lattice) are given and compared against state-of-the-art NoC solutions [Mai15] and [Pap15]. RingNet achieves a higher clock frequency and uses less resources than [Mai15] and [Pap15]. It would have been interesting to also include the latency from the simulation chapter into this comparison.

Chapter 9: RingNet is compared against AXI4 Interconnect in terms of maximum clock frequency and resource utilization, which is the state-of-the-art FPGA communication infrastructure. The target FPGA used is an Artix7 from Xilinx. RingNet achieves a higher clock frequency and uses less resources than the AXI Interconnect.

Chapter 10: Conclusions and future directions summarizes the main achieved results and shows the potential of next steps.

Besides theoretical aspects and concepts in the thesis a practical realization including simulation and synthesis results of RingNet are presented and compared against the state-of-the-art in this domain. Mr. Siast shows with his work the important combination of scientific work and practical realization. This is underlined with 1 publication at a highly ranked international journal (IEEE Transactions on VLSI). Mr. Siast has a strong background in multimedia applications and their realizations on FPGAs, which is proven with the impressive number of 34 publications. It would have been interesting to see the combination of both, i.e. a practical realization of RingNet in such memory-oriented SoCs within the thesis. In Chapter 7 this was shortly mentioned by citing [Dom15], but a stronger elaboration within the thesis would have been interesting, especially due to his previous publications in this field.

In summary, Mr. Siast shows with this dissertation and with his publications that he is able to address a complex research topic in depth within the time frame of a PhD thesis. Therefore, I recommend the Poznan University Technology to accept this thesis and to proceed with the oral defense.

Yours sincerely,

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