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Review

of the doctoral thesis prepared for
the Faculty of Electronics and Telecommunications
of Poznan University of Technology

Title: On a New Class of Test Points and their Applications

Author: Justyna Zawada

The research problems addressed and methodology employed in the thesis: This thesis is primarily aimed at enhancing the efficiency of industrial integrated circuit (IC) test methodologies by improving the design-for-test circuitry that is built into ICs to support testing. More specifically, the thesis develops new algorithms for selecting the locations where test points are inserted into the circuit. Such test points improve the ability of the test programs to more easily control internal circuit signals (set them to desired logic 0 or logic 1 values), thereby allowing the effects of faults buried deep in the circuitry to be readily observed at the circuit outputs.

The thesis takes an entirely new approach to test point insertion than is currently employed. The proposed new approach focuses on minimizing conflicts between the internal signals needed to allow the simultaneous detection of any one of the many possible internal faults by a single test pattern (one set of inputs applied to the circuit). This reduces the number of test patterns that must be applied to detect all possible faults in the circuit, thereby reducing test application time and test costs. The basic signal conflict minimization approach developed in this thesis is further used to design new and more effective algorithms for test point insertion in a number of different applications. These include design-for-test architectures such as the widely employed EDT, Logic BIST, and a proposed new test-per-cycle BIST presented here. Finally, it is also shown how the test points can be exploited to obfuscate the logic functionality of the circuit for hardware security applications.

This thesis is extremely well written, with problems clearly formulated and the proposed solutions described in detail with the help of examples. The work is both theoretical and experimental; the concepts and algorithms developed have been applied to real industrial designs and extensively evaluated through simulation using state-of-the-art industrial CAD tools.

Literature review and context of the work relative to the state-of-the-art and industrial practice: The research performed in this thesis has been carried out in close collaboration with the leading EDA company in the area of IC testing. The student was on a Mentor Graphics scholarship during her Ph.D.

and interacted extensively, not only with Mentor experts in Poland and the US, but also with those from Intel and Broadcom. As a result, she displays excellent understanding of state-of-the-art solutions and relevant industrial applications, at a level that is exceptional for most Ph.D. students. The technical contributions in the thesis are innovative and show excellent results in terms of improved circuit testability. The conclusions drawn are clear, convincing, and highly relevant to industrial practice. Any assumptions made have been extensively vetted in an industrial environment and are therefore quite credible.

Originality of the contributions of the thesis: Test point insertion has traditionally been investigated in the past in the context of BIST, where the primary aim is to improve and maximize test coverage for the limited set of test patterns that can be efficiently generated on-chip. This thesis, for the first time, considers test point insertion where there is no (or minimal) restrictions on the test patterns that can be used. In such an environment, the highest possible coverage can always be achieved by using custom ATPG generated test patterns. However, the aim of the new class of test points developed in this thesis is to achieve this coverage using the fewest number of test patterns so as to minimize the required test application time. This different objective calls for completely different test point placement, where the focus now is on reducing signal conflicts that prevent multiple faults to be detected by the same test pattern.

Note that advanced semiconductor technology nodes, with new structures such as FinFETs, exhibit many new failure modes that must be reliably detected during testing. This has resulted in an explosion in the number of test patterns needed to detect all possible faults. Consequently, test application time has become a very serious practical concern. This is the first work that I have seen that provides a truly practical solution by significantly reducing the pattern counts needed by a factor of 2X or more.

Weak points and drawbacks of the thesis: Any weaknesses that I see in the thesis come from my own desire to see even more detailed results because this is such good work, which has been further validated with industrial strength experiments. It would have been interesting, for example, to explore pattern count reduction for varying test point insertion overhead, starting with the least possible overhead -only functional test points and no observation points. However, there is more than ample research reported in the thesis, and such further work can be the subject of future research.

Practical application of the results and significance of the research: The results from this thesis can be quickly and directly used in practice. For example, the biggest obstacle limiting the use of Cell Aware test methodology, which has been shown to significantly improve test quality, is the near doubling of test pattern counts. The proposed test point insertion methodology can easily reduce pattern counts by a factor of two or better. Thus, when used in conjunction with Cell Aware tests, it can ensure no net increase in pattern counts and test time, while delivering much better test quality.

Meanwhile, logic BIST is also seeing significant demand in the automotive and other high reliability application areas. The proposed hybrid test point insertion approach presented in this thesis can greatly improve the effectiveness of LBIST and promote this emerging application.

Thus, the results from this thesis are likely to have an immediate and significant impact in improving the capability of IC test methodologies, particularly since the major commercial companies are already aware of this research.

Overall rating of the thesis: This thesis is easily amongst the best that I have read in recent years. It certainly fulfills requirements for the degree of Doctor of Philosophy, and deserves the highest distinction due to its award quality.

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